2.5/3D Packaging NEPP ETW

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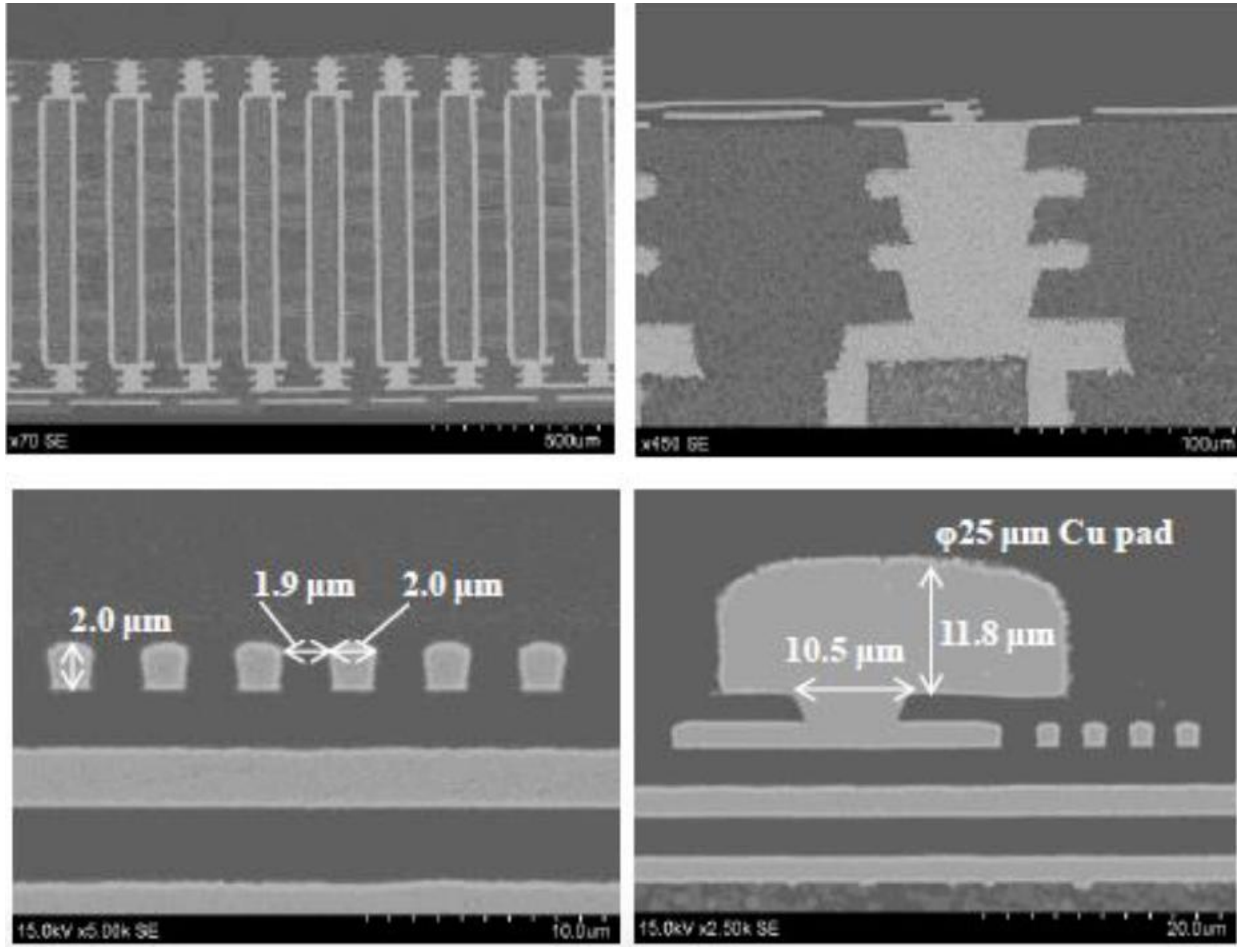
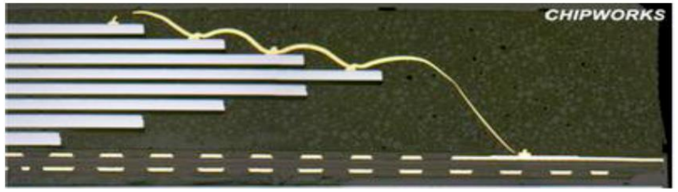
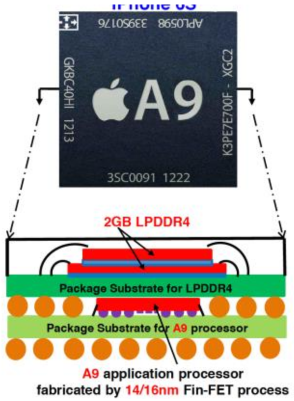


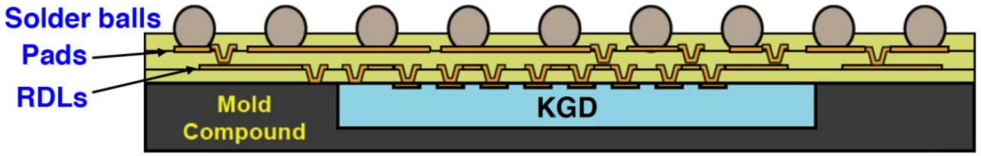
Overview - Review today's agenda

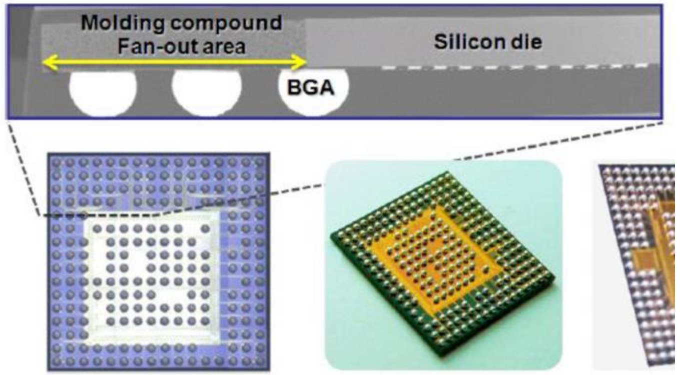
- Discussion of NEPP 2.5/3D – Sheldon
  - Provide background, technology roadmaps, overview of NEPP products/deliverables
- *"Statistics and Physics in Reliability"* – Lloyd
  - A rigorous and foundational understanding of physics and statistics is needed to address the reliability problems of 2.5/3D packaging technology.
- NEPP Packaging Tasks – (Popelar, Suh, Ghaffarian)
  - Updates on current results
- DTRA 3D Packaging – Alles
  - Radiation effects in complex structures with >50% High Z materials
- 2.5/3D Roadmaps and OSAT Advanced Packaging
  - Commerial growth and development of these technologies is continual and expansive. Need SOA industry partners to provide guideance and direction on options for NASA

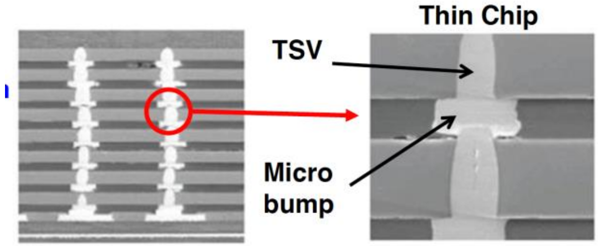
The ever changing world of packaging

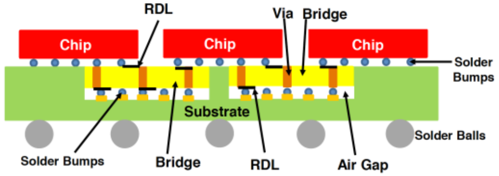


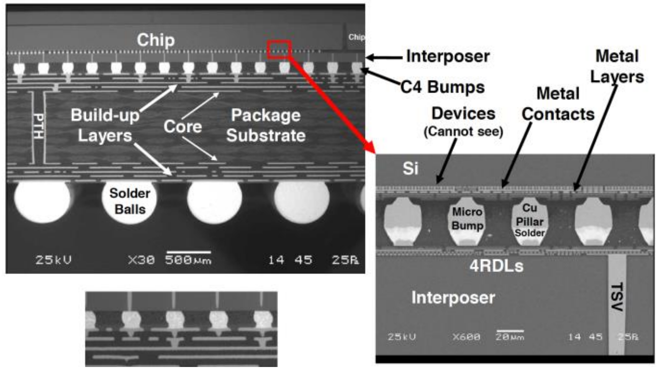


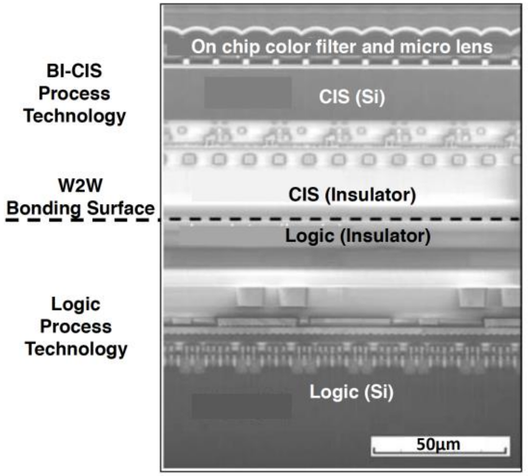


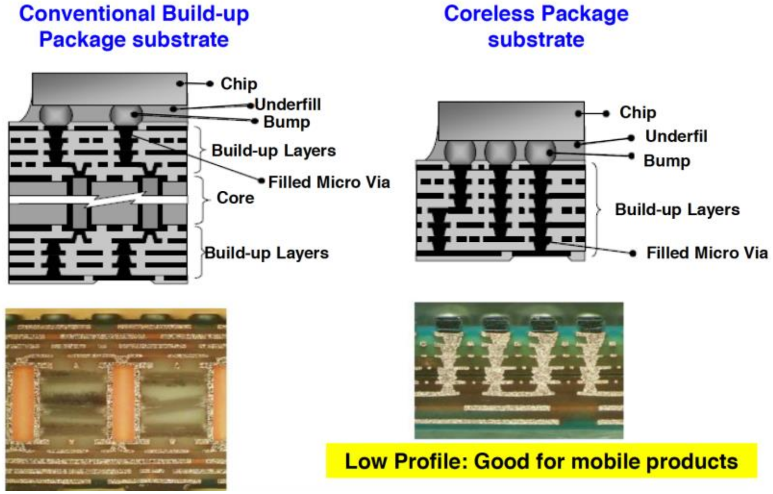




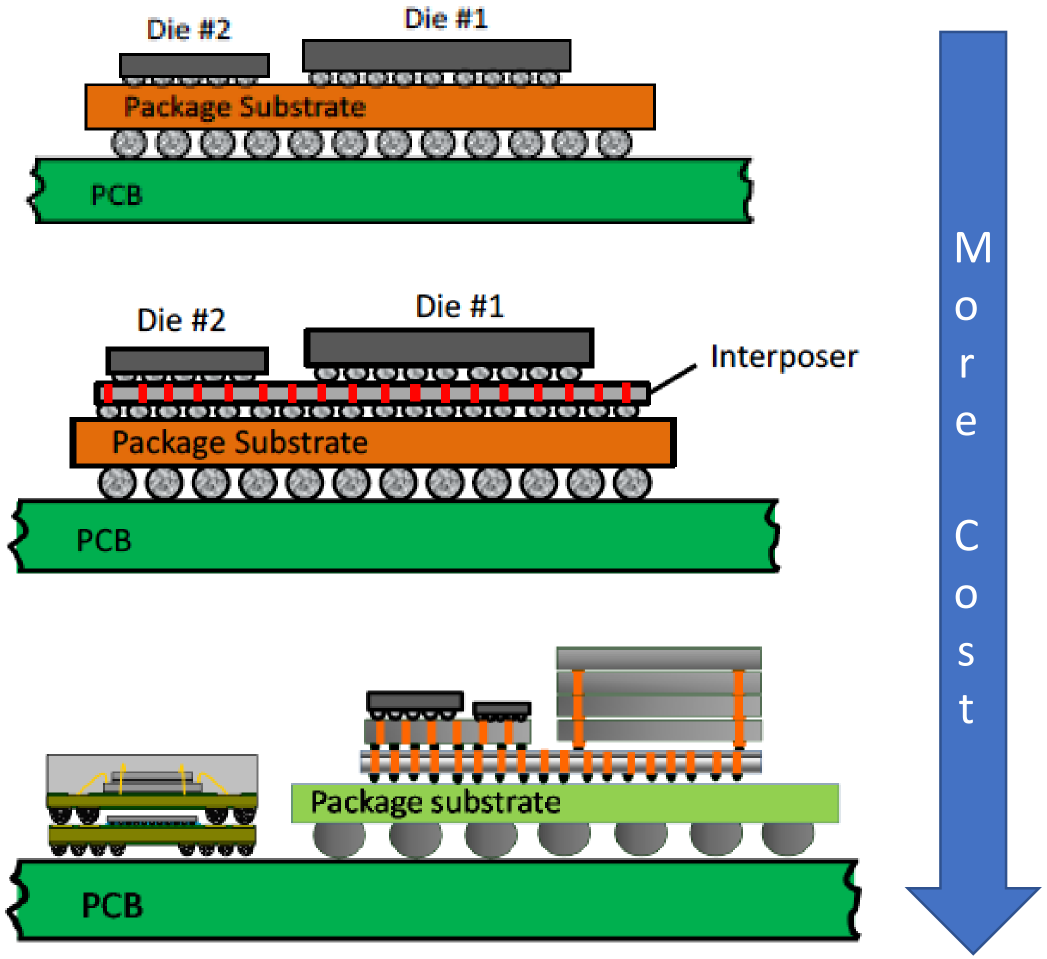








2D to 2.5D to 3D

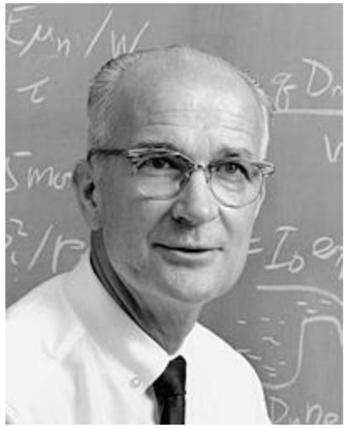


- 2D is one or more die mounted in a single plane
- 2.5D consists of one or more die mounted on an intermediate interposer and then mounted onto the package substrate
  - Interposer can be:
    - Silicon
    - Glass
    - Ceramic
    - Organic
- 3D has many different combinations and options
  - Package-on-package
  - Stacked die with wire bond
  - Stacked die with wire bond and flip chip
  - Stacked die with TSV
  - Stacked die utilizing intermediate interposers

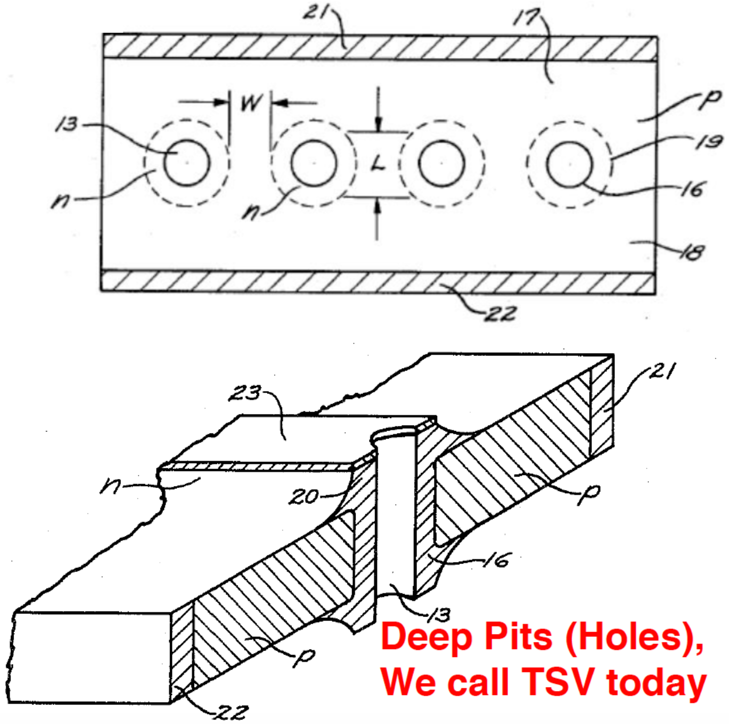
3D Packaging is a new technology! (Not)

TSV (Through-Silicon Via)

William Shockley (co-invented the transistor) filed a patent, "Semiconductive Wafer and Method of Making the Same" on October 23, 1958 and was granted the US patent (3,044,909) on July 17, 1962.



William Shockley
(1956 Nobel laureate)



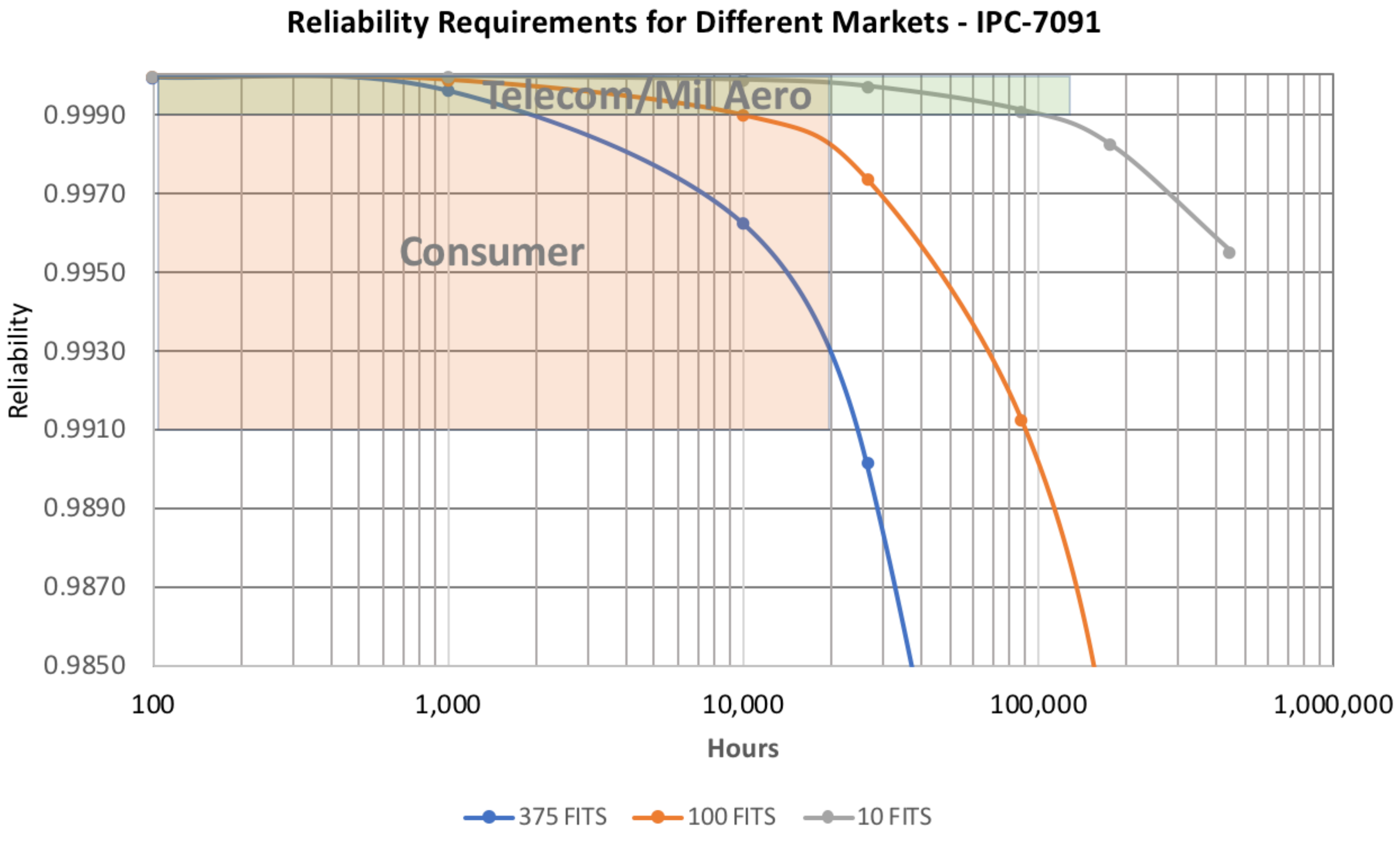
Deep Pits (Holes), We call TSV today

- Conceptually the idea of joining different devices together is very appealing and has been around for a long, long time.
- Only through the maturization of modern wafer and manufacturing processes has it finally become a reality

COTS, COTS, and COTS…

- 2.5/3D package technologies are driven by needs to shrink size, reduce weight and improve performance. (SWaP)
- ***NOT to improve reliability***
- COTS = Commerical and often ***Consumer*** Off the Shelf Technologies
- ***Consumer*** = limited life expectancy, planned obsoloence
- Unless ***very explicitly designed*** from the ground up, these technologies are expected to have at best break even reliability compared with heritage Plastic Encapsulated Microcircuits (PEMs) and more likely to have worse reliability.
- *This implies any use on NASA missions would require significant upscreening and qualification*.

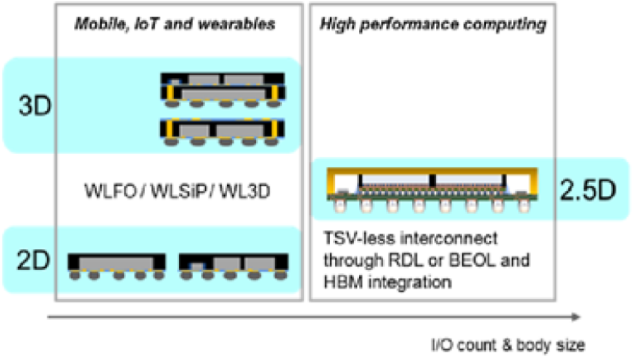
Reliability requirements for different markets

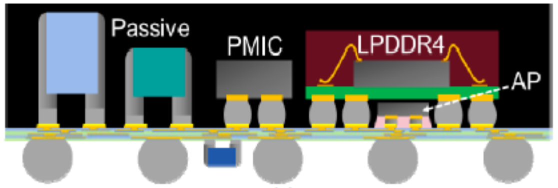


What different FIT rates mean graphically

Example of Concerns – 2.5/3D Packaging – IRPS 2018

- **High-Density Fan-Out Technology for Advanced SiP and 3D Heterogeneous Integration – Lee (Amkor)**
  - FOWLP is divided into low-density and high-density by I/O density and multi-functionality.
    - Low-density fan-out package has core structure composed of 1~2 layers Cu RDL with 8~15um.
    - High-density fan-out package has 3~4 layers Cu RDL with 1~5um width. Demand is expected to increase significantly
  - Two options:
    - wafer-level system-in-package (WL-SiP)
    - 3D heterogeneous integration (3D SWIFT)
      - 3D SWIFT can bond top dies directly onto the mold sidevRDL of bottom fan-out packaging layer
      - 3 layers RDL with 5~10um width and Cu posts are formed on a carrier substrate
  - ***Biased HAST showed that 4/4um L/S Cu RDL meets the JEDEC 200 hours / 130°C / 85%RH /3.5V - 2/2um and 1/1um L/S Cu RDL dropped rapidly immediately after the biased HAST started***.
  - change in the insulation resistance is strongly correlated with the intensity of the electric field generated between the Cu RDL.
  - Cu migration into the organic dielectric
  - New dielectric barrier layer required below 2um L/S.





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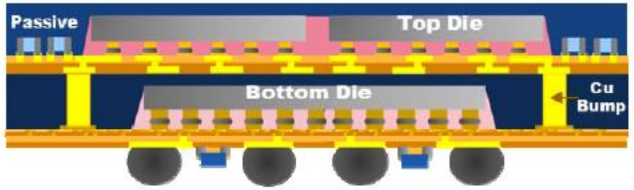
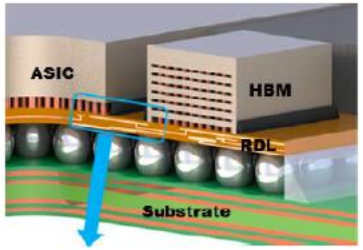
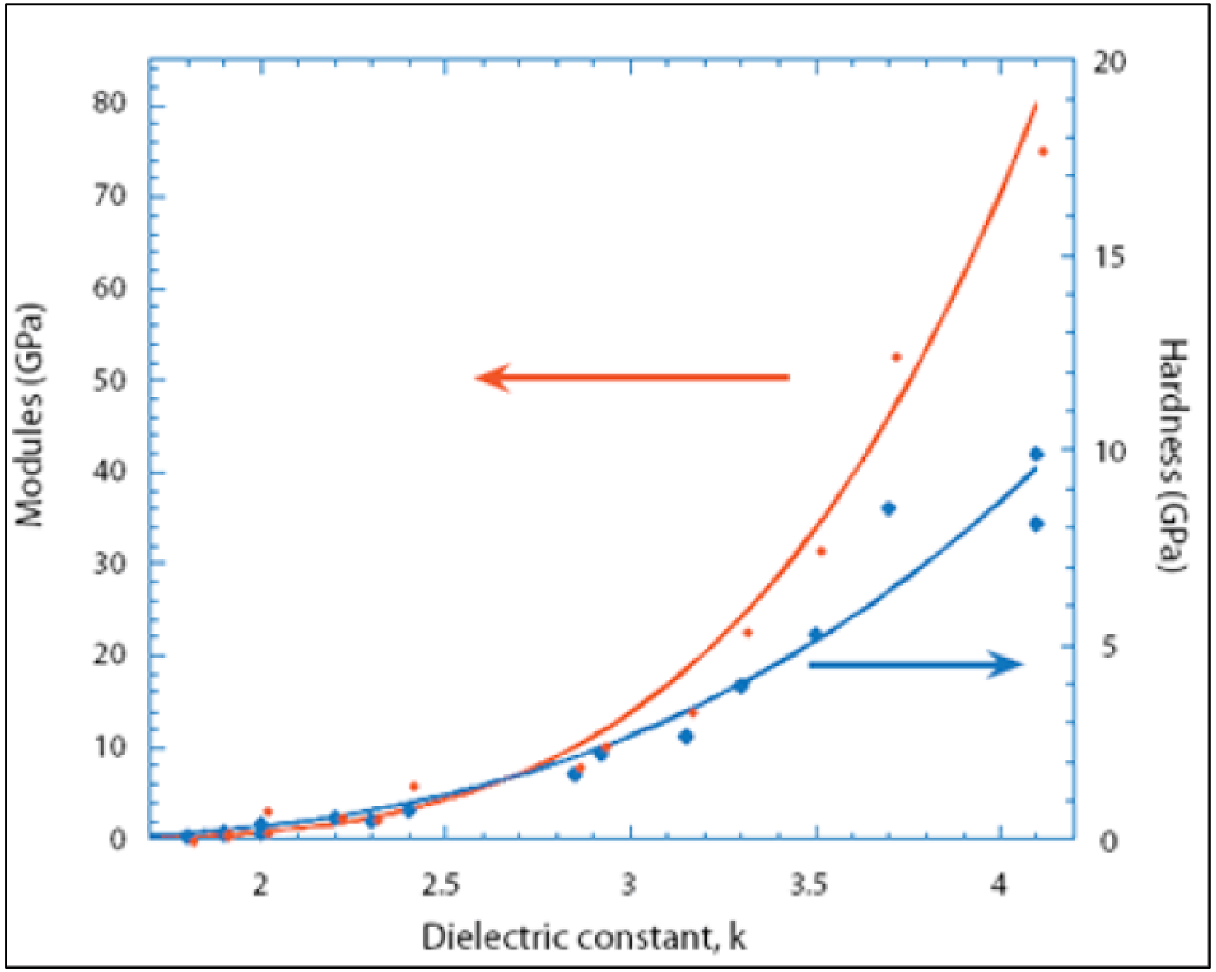




Low dielectric constant materials needed for high density interconnections



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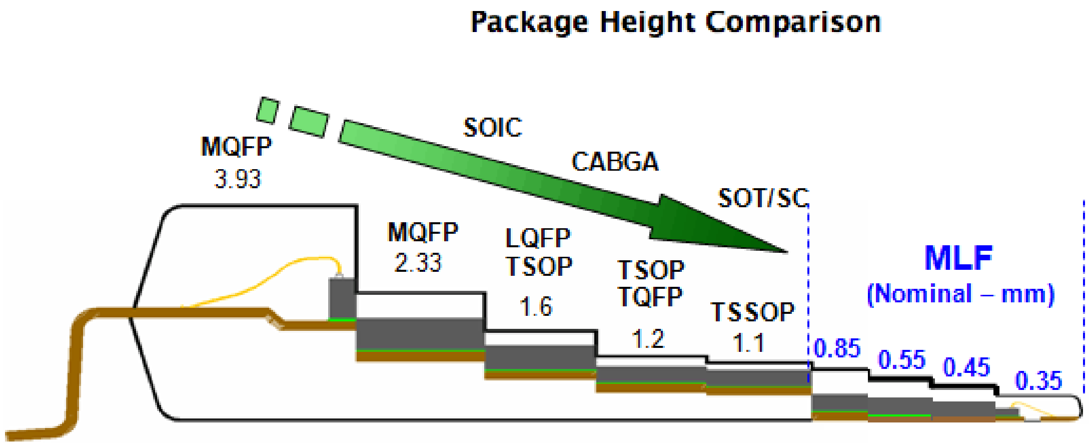
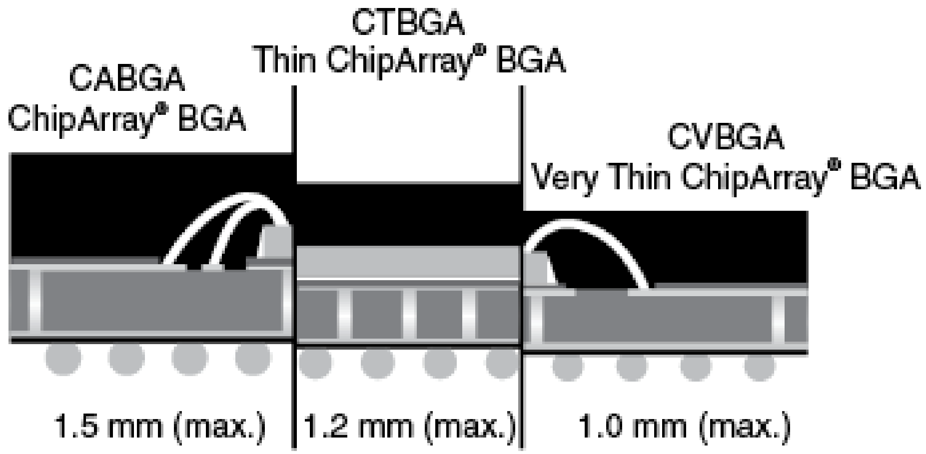
Dielectric Film	k	Pore %	E (GPa)	H (GPa)
Non-porous OSG	2.8	0	8.7	1.59
Porous OSG A	2.2	45	3.1	0.57
Porous OSG B	2.0	50	0.9	0.14
Porous OSG C	1.8	60	0.5	0.07
Non-porous Polymer	2.7	0	3.2	0.19
Porous Polymer	2.2	15	1.1	0.11

- Ultra low dielectric films can be >60% porus!

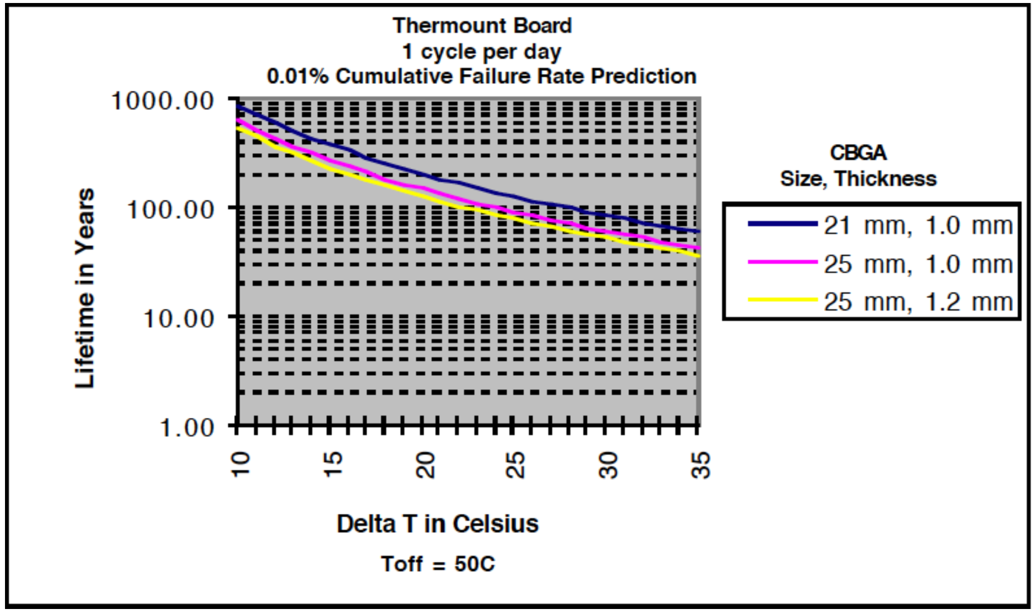
Thickness scaling of COTS packaging





- Extreme thickness scaling is required for modern cell phone applications

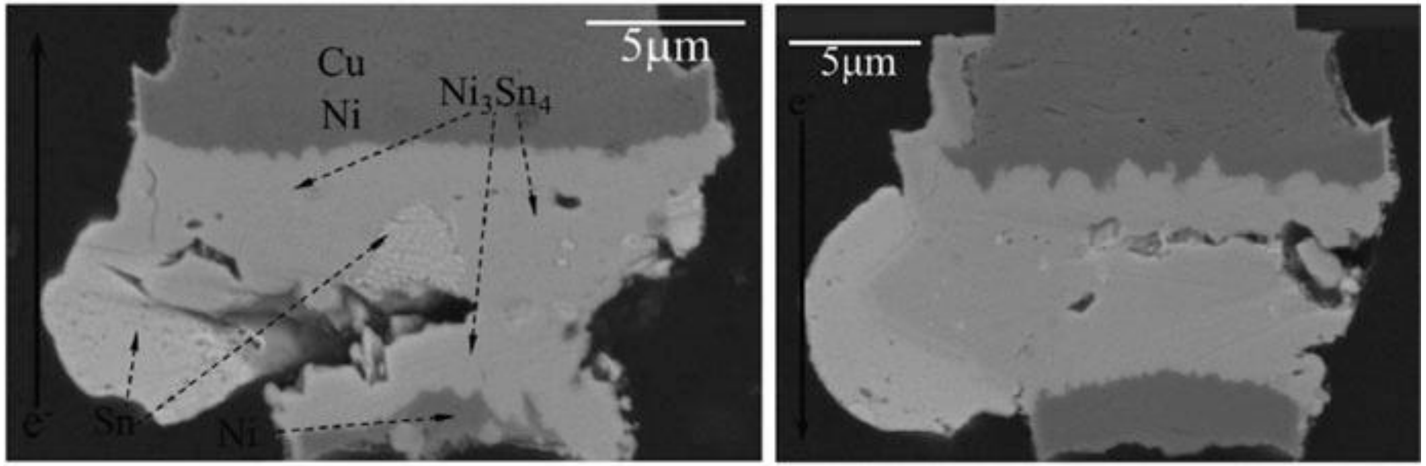
- 25% difference in lifetime with 20% change in thickness
- Independent of temperature stress

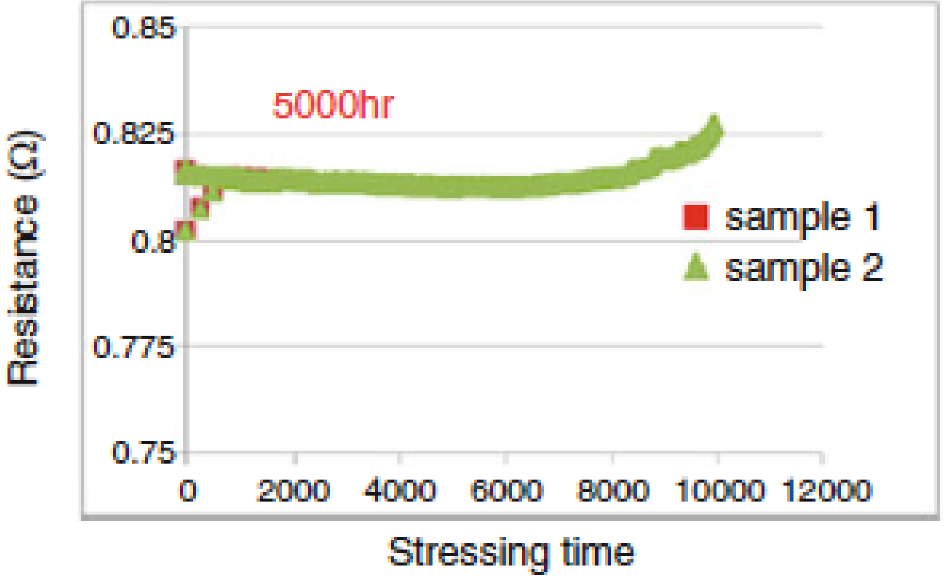


Unique EM results in Microbumps

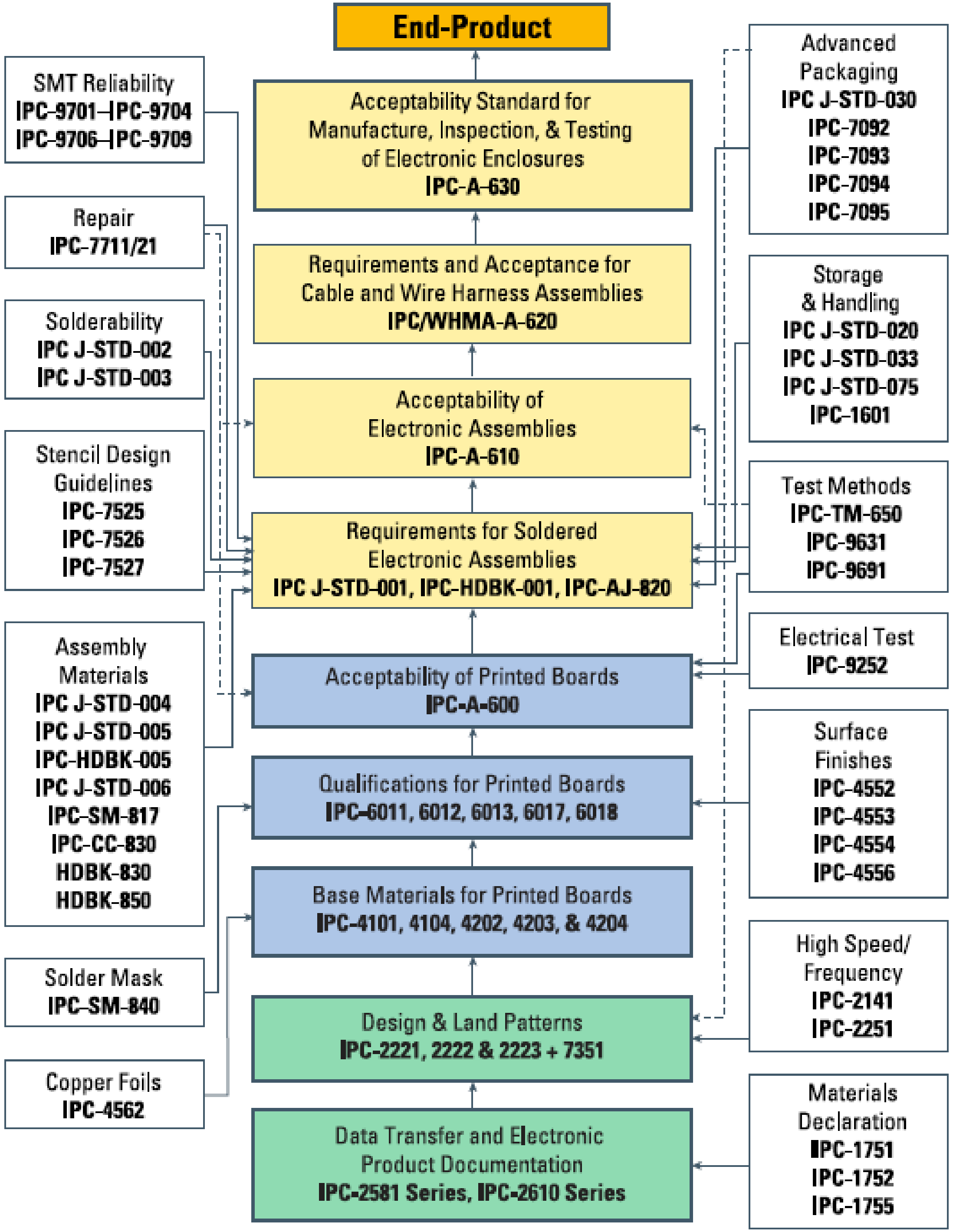
$$\frac{1}{\mathrm{MTTF}} = A\left(j - \frac{(jL)_c}{L}\right)^n \exp\left(-\frac{Q}{\mathrm{RT}}\right)$$

- Compared with larger solder joints in C4 flip chip and BGA packaging, unique EM behaviors happen in micro bumps of 3D packaging due to their smaller dimensions
- Back Stress in Blech effect for short micro bumps is high enough to dramatically delay or eliminate the EM damage caused by Sn flux divergence
- It typically has smaller solder to metallization volume ratio, which can form a full IMC bump before the metallization is fully consumed





Specifications to Support Qualification



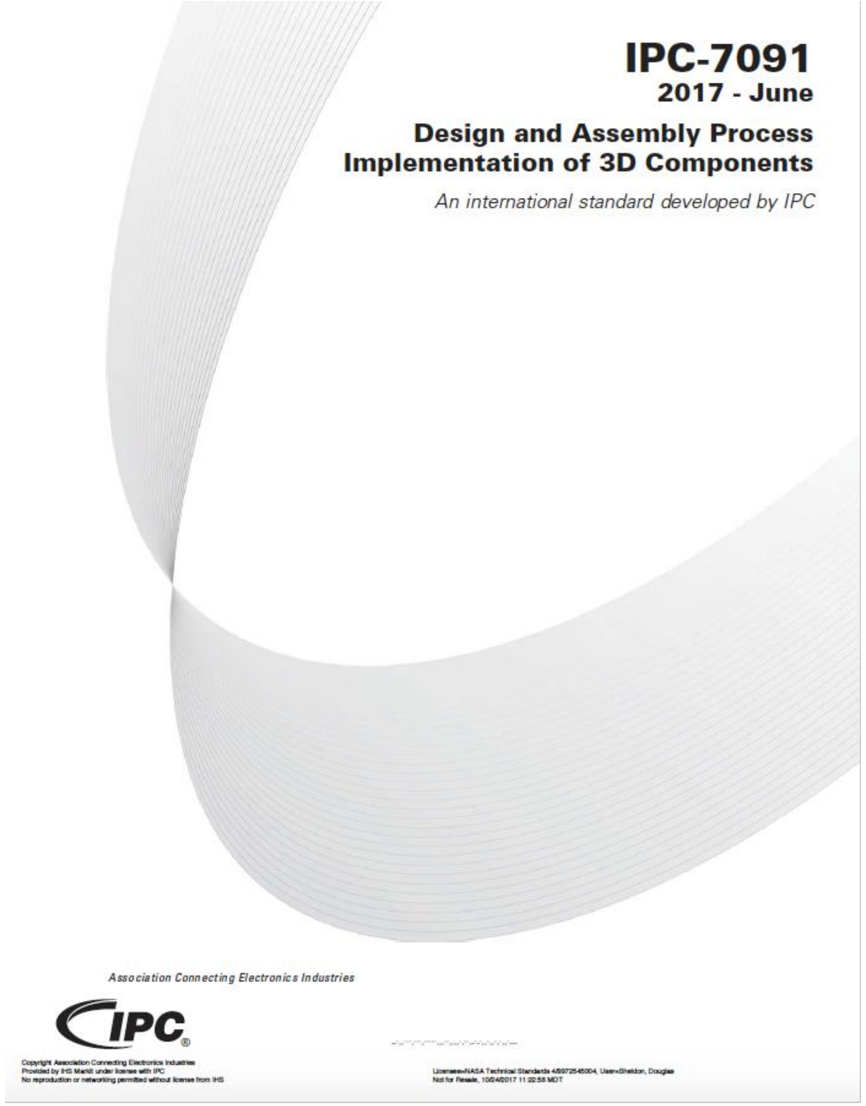
Existing Specifications – IPC Standard Overview

NEPP Packging Focus

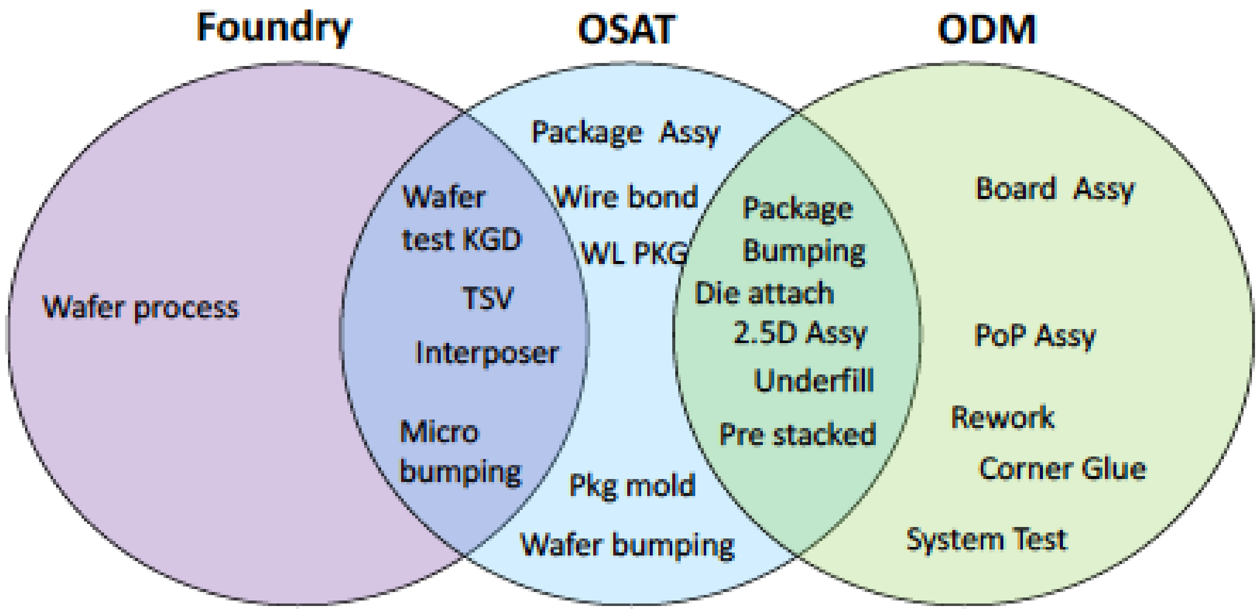
Doc #	Title	Comment
IPC-7091	Design and Assembly Process Implementation of 3D Components	IPC-7091 is the main reference document. However the other four documents represent important technology building blocks and previous generations. Reference to these for additional insights
IPC-7092	Design and Assembly Process Implementation for Embedded Component	
IPC-7093	Design and Assembly Process Implementation for Bottom Termination SMT Components	
IPC-7094	Design and Assembly Process Implementation for Flip Chip and Die Size Components	
IPC-7095	Design and Assembly Process Implementation for BGAs	

IPC-7091 Design and Assembly Process Implementation of 3D Components

1. General Terms
2. Device Considerations
3. Interposer/Substrate Materials
4. Process Materials
5. Package Level Standardization
6. PWB Mounting Base/Stackup Considerations
7. Design Methodology
8. Assembly of 3D Packages on PWB
9. Testing and Product Verification
10. Reliability
11. Defect and Failure Analysis
12. Supplier Selection and Qualification



IPC-7091 View of 3D Packaging World*



- *"The next generation of 3D assembly has many implementation challenges*
- *The technology is complex and requires process expertise that may require*
  - *Foundries*
  - *Outsourced Semiconductor Assembly and Test (OSAT) providers*
  - *Original Design Manufacturers (ODM).*
- *There is no clear direction where 3D packages will be built, tested and assembled.*
- *The type of process to be used and the order of assembly and stacking is not defined and depends on the assembler's expertise".*

COTS use JEDEC standards

- Qualification
  - JESD47, Stress-Test Driven Qualification of Integrated Circuits
  - JESD94, Application Specific Qualification Using Knowledge Based Test Methodology
  - JEP148, Reliability Qualification of Semiconductor Devices Based on Physics of Failure and Risk and Opportunity Assessment
  - JEP158 3D- Chip Stack With Through-Silicon Vias (TASVs): Identifying, Evaluating and Understanding Reliability Interactions
- Model Development
  - JEP122, Failure Mechanisms and Models for Semiconductor Devices
  - JEP126, Guideline for Developing and Documenting Package Electrical Models Derived from Computational Analysis
  - JEP132, Process Characterization Guideline
  - JESD90, Method for Developing Acceleration Models for Electronic Component Failure Mechanisms
- Failure Rate
  - JESD37, Standard Lognormal Analysis of Uncensored Data, and of Singly Right -Censored Data Utilizing the Persson and Rootzen Method:
  - JESD63, Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature
  - JESD74, Early Life Failure Rate Calculation Procedure for Electronic Components
  - JESD85, Method of Calculating Failure Rates in Units of FITs

Package Qualification Tests – COTS ”Black Box”

Package Qualification Reliability Tests:

Resource Name	Stresses
Preconditioning	Reflow (240°C to 260°C), 3X
Hammer test	Reflow (240°C to 260°C), 1X, 5X, 10X, 15X, 20X
Quick Temperature Cycling	–40°C to +60°C, 1X, 10X, 20X, 40X
Thermal cycle	Conditions (B: –55°C to +125°C, G: –45°C to +125°C)
HAST	Bias HAST, HAST 130°C, 85% RH
Thermal shock	Thermal Shock (B, G), X cycles
Temperature Humidity	TH Bias, TH 85°C, 85% RH
High Temperature Storage	150°C, 1000 hrs
Board Level Reliability	Thermal Cycle, Shock test, Bend test, Vibration test

- Typical qualification based approach to testing
- 0 failure expected
- Provides generic reference point to compare to other technologies
- Begin to estimate Physics of Failure distributions and possible FIT rates

What might be missing? Test data from manufacturer

- Pre-bond interposer testing
  - Interposer cannot be tested (easily) before it is stacked with other die.
  - Requires both horizontal and vertical interconnection testing
  - Need strategy to for test connections that might not be device connections
- At speed testing
  - Use of IEEE 1149.1 TAP and BIST
  - Multiple metal layers can influence capture and update cycles due to clock variation
    - Hard to detect small delay defects
- High density I/O and Interconnects
  - Interposed can have >10K die to die interconnetions with as many as 1,500 I/O ports
  - 2.5D IC can have 25K C4 bumps but 250K microbumps!
  - Majority of I/O pins are connected to other die through interposer, not to external world

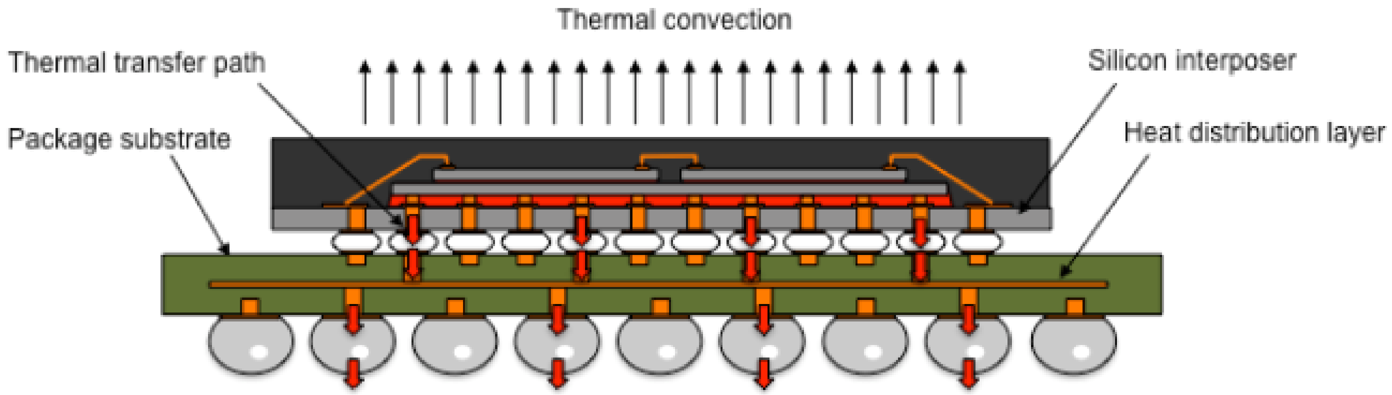
Formalism for Evaluation – 1/2

- 2.5/3D packaging technology represents a new scaling approach way EEE parts technology (vs. Dennard transistor scaling)
- Scaling implies shrinking dimensions, increasing electric field, and changing materials.
- Just as with transistors – similar reliability concerns/formalisms
- Mechanical failures usually dominate in packaging
  - Mismatch of TCE -> stress cracking under temperature cycling stress
- Electrical failures also must be considered
  - Electromigration (particularly from bumps)
  - Dielectric breakdown is also concern – certainly for new materials w/ ULK materials

Formalism for Evaluation – 2/2

- Daisy Chain packages offer simplest approach
  - Easy to determine failure location for DPA/FA
  - Often not available in state of the art, sophisticated technologies however
- Custom test devices sometimes available
  - Need collaboration with industry/partners
- Final product testing also required
  - Often the only way to get precise technology
  - Leverage vendor data and independent evaluation

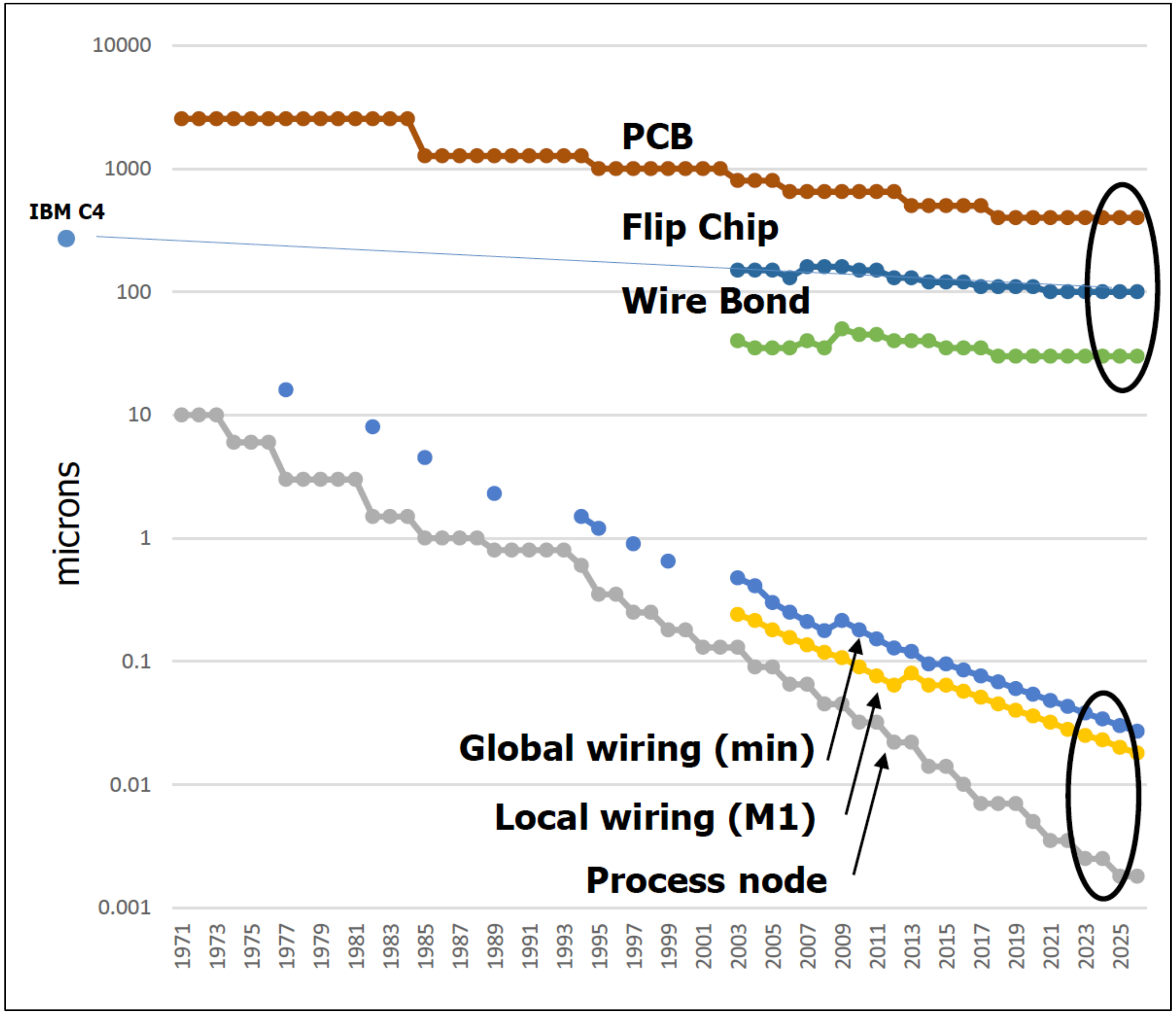
Thermal Modeling and Measurement – A Best Practice



- Stacking multiple active device or packaging layers proportionally increases heat dissipation rates per unit volume
- New dielectric layers with low thermal conductivity that exist between chips can lead to high temperatures.
- Heat is the single biggest cause of failure in electronics.
- Reducing the operating junction temperature by as little as 10 °C can double a device’s lifetime
- Managing thermal dissipation remains a primary challenge for multiple-die, configured components
    - Heat pipes
    - Liquid
    - Microchannels

Technology Roadmaps

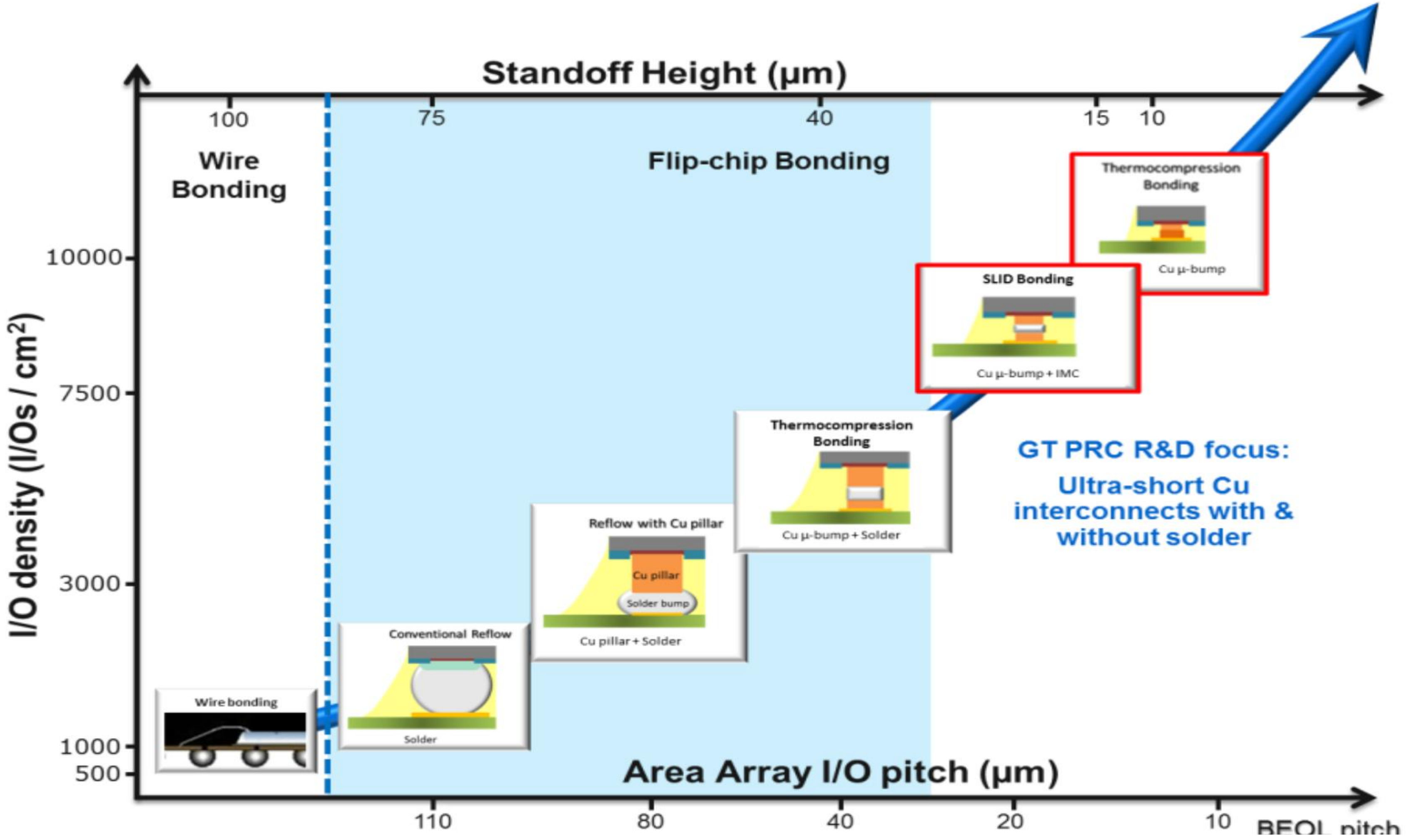
Package Technology Scaling vs. Wafer



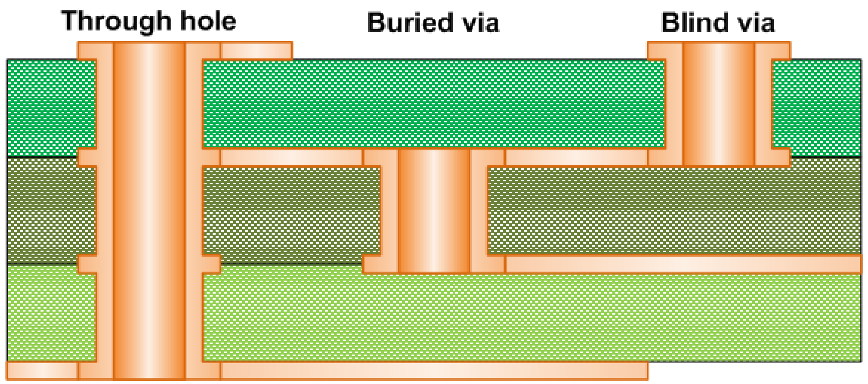
- Interposer and TSV bridge the gap in dimensions between heritage packages and wafer fab device dimensions

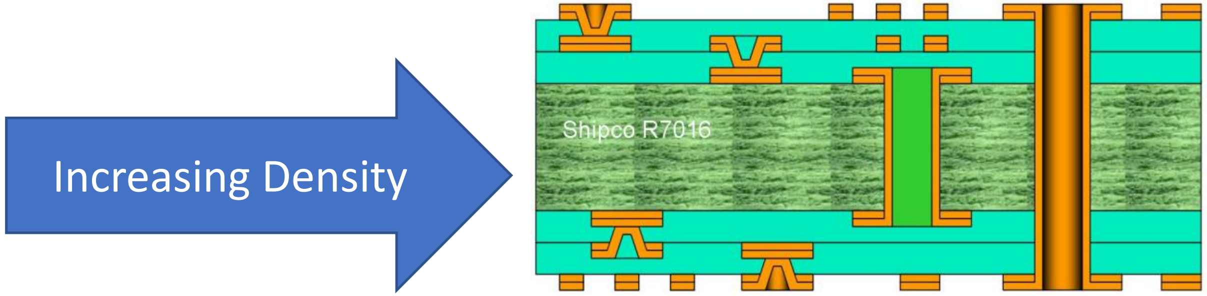
DARPA CHIPS

Scaling roadmap – I/O pitch, density and standoff height



Substrates play a critical role in 2.5/3D Packaging



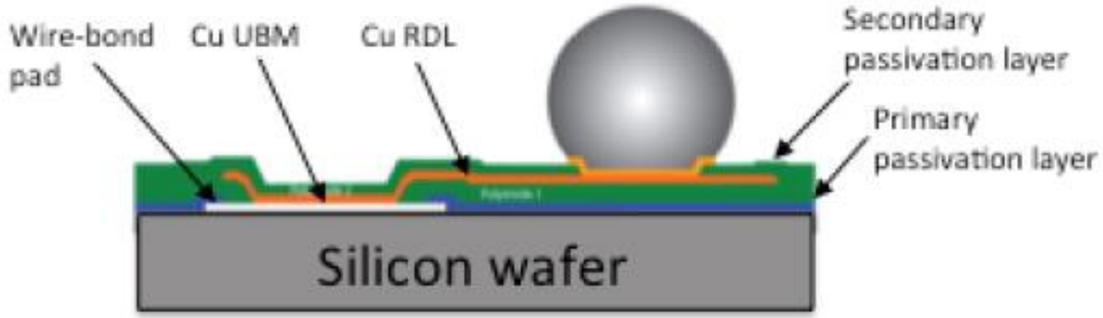


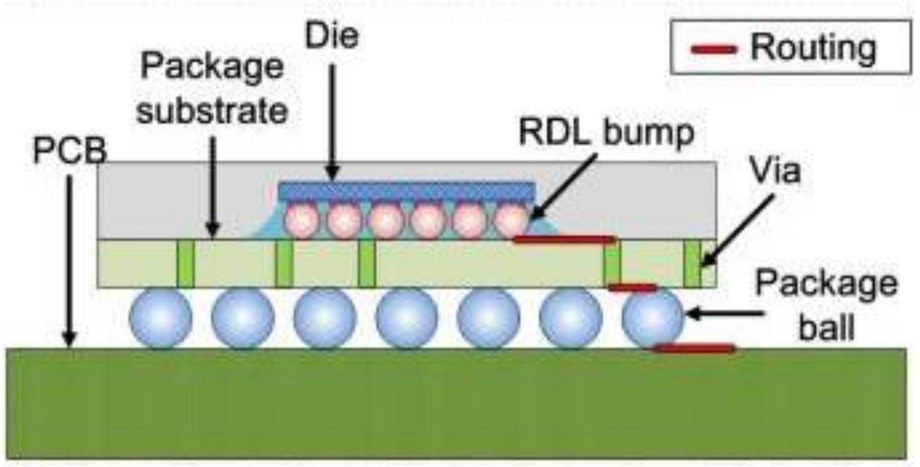
High Density Interconnect (HDI)
Substrate with Micro Vias

Standard (Epoxy Glass or Polyimide)	**HDI: Dense** (Particle Filled Epoxy)	**HDI: LCP** (liquid crystal polymer)	**HDI: PTFE** (PTFE)

- Dielectric materials, etch processes, and interconnect dimensions drive reliabilty

Redistribution Layers (RDL)





- The redistribution layer (RDL) is the interface between chip and package for flip-chip assembly
- Used in flip-chip designs to redistribute I/O pads to bump pads without changing the I/O pad placement
- the chip that enables you to bond out from different locations on the chip, making chip-to-chip bonding simpler.
- The RDL process is performed following basic copper UBM plating. Redistribution employs an additive copper plating process following a passivation process that covers the active surface of the die (Figure

Packaging Technologies are Driven by End Market

	Mobile	IoT	RF	Automotive	Computing	Networking	Storage
QFN		●	●	●			
FBGA		●	●	●			
WLCSP		●	●				
FOWLP	●	●	●	●			
SiP	●	●	●	●			●
fcCSP	●		●	●			
FCBGA				●	●	●	
2.5D					●	●	
3D					●	●	
Si-PH					●	●	●

- Note many different package technologies needed for Automotive, RF and IoT markets.
- NASA applications can leverage these different technologies but need to be aware of market expectations.?

NEPP Package Testing Summary

		Package Type														
		TC_BGA	CA_BGA	CV_BGA	FCV_BGA	CSP	PBGA	FCBGA	LGA	QFN	TMV	TSV	Wafer Level	Stacked Silicon Interconnect (SSI)	Flip Chip w/ Organic Substrate	Cu Pillar
Testing Conditions	Daisy Chain	Y	Y	Y		Y	Y	Y	Y	Y	Y		Y		Y	Y
	Product				Y				Y			Y		Y		
	-55 to 100C/ 200 cycles									Y	Y		Y			
	-55 to 100C PoF TC									Y					Y	Y
	80C bake											Y		Y		
	200cycles/-55C to 125C + 200 cycles/-65C to 150C	Y	Y	Y	Y	Y	Y	Y	Y			Y				
	Custom JPL assembly protocol															
	HALT protocol		Y	Y		Y	Y	Y								

Jet Propulsion Laboratory
California Institute of Technology

jpl.nasa.gov